UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,996	12/26/2000	Shoji Goto	001717	1382

38834 7590 10/13/2004

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP
1250 CONNECTICUT AVENUE, NW
SUITE 700
WASHINGTON, DC 20036

EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 10/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,996	GOTO, SHOJI	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *9* is/are allowed.

6)☐ Claim(s) *4 and 12* is/are rejected.

7)☐ Claim(s) *1-3,5-8,10,11,13-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-16 are pending in the instant application.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on July, 29 2002 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement, **including reference AF**, is being considered by the examiner.

Response to Amendment/Arguement

3. Applicant's arguments, see page 21, filed June 29, 2004, with respect to the 35 U.S.C §112 first paragraph rejections of claims 4, 7, 8, 12, 15, and 16 have been fully considered and are persuasive in view of the amendments to the claims. The rejections of claims 4, 7, 8, 12, 15, and 16 set forth in the first office action have been withdrawn.

However, new rejections have been made.

Claim Objections

4. Claims 1-3, 5-8, 10, 11, and 13-16 are objected to because of the following informalities:

Regarding claim 1, the limitations of the first and the second product-sum calculating means are objected to because they do not clearly embody the invention. Particularly, the first and remaining part of the received signal and the corresponding first and remaining part of the generated spreading sequence are not clearly grouped together for use in the first and second product-sum calculating means. It is suggested that the paragraphs in claim 1 relating to the first and the second product-sum calculating means are amended as follows (or equivalently):

first product-sum calculating means for calculating a correlation value between a part of the predetermined number of samples held in said received signal holding means and a part of the generated spreading code sequence ~~spreading codes~~ corresponding to said part of the predetermined number of samples ~~in said generated spreading code sequence~~ held in said received signal holding means,

second product-sum calculating means for calculating a correlation value between a remaining part ~~number of samples~~ of the predetermined number of samples held in said received signal holding means and a remaining part of the generated spreading code sequence ~~spreading codes~~ corresponding to said remaining ~~number of samples in said generated spreading code sequence~~ part of the predetermined number of samples held in said received signal holding means, and

Regarding claims 3, 6, 8, 11, 14, and 16, the claims are nearly indefinite because the relationship between the logic circuits and the storage circuits is unclear in reference to the load capacitance. It is unclear if the load capacitance of one logic circuit is smaller than the load capacitance of the one respective storage circuit it is coupled to or the capacitance of all the storage circuits collectively. Further, the measure of load capacitance may be interpreted to be an input or an output load capacitance and should be amended to be more definite.

Appropriate correction is required.

Regarding claim 2, the limitation "said predetermined number of logic circuits" in line 16 should be replaced by –said logic circuits--.

Regarding claim 5, the limitation "said part of samples in said generated spreading code sequence " in line 30 should be replaced by –a corresponding part of samples in said generated spreading code sequence--, and "said rest of samples in said generated spreading code sequence" in line 33 should be replaced by –a rest of samples in said generated spreading code sequence--.

Regarding claim 7, the limitation "said part of samples in said generated spreading code sequence " in line 33 should be replaced by –a corresponding part of samples in said generated spreading code sequence--, and "said rest of samples in said generated spreading code sequence" in line 36 should be replaced by –a rest of samples in said generated spreading code sequence--.

Regarding claim 7, the limitation "said predetermined number of logic circuits" in line 17 should be replaced by –said logic circuits--.

Regarding claim 10, the limitation "said predetermined number of logic circuits" in line 22 should be replaced by –said logic circuits--.

Regarding claim 13, the limitation "said part of samples in said generated spreading code sequence " in line 36 should be replaced by –a corresponding part of samples in said generated spreading code sequence--, and "said rest of samples in said generated spreading code sequence" in line 39 should be replaced by –a rest of samples in said generated spreading code sequence--.

Regarding claim 13, the limitation "said predetermined number of logic circuits" in line 22 should be replaced by –said logic circuits--.

Regarding claim 15, the limitation "said part of samples in said generated spreading code sequence " in line 40 should be replaced by –a corresponding part of samples in said generated spreading code sequence--, and "said rest of samples in said generated spreading code sequence" in line 43 should be replaced by –a rest of samples in said generated spreading code sequence--.

Regarding claim 15, the limitation "said predetermined number of logic circuits" in line 23 should be replaced by –said logic circuits--.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 4 is rejected under 35 U.S.C. 102(b) as being anticipated by Leibowitz (US 4660164).

Regarding claim 4, Leibowitz discloses by figure 2 a digital matched filter (correlator) for despreading (correlating) on reception side a received signal sequence ("DATA") having been spread on transmission side (abstract), comprising: received signal holding means (refs. S1-S16) for successively holding a first predetermined number of samples among samples constituting said received signal sequence input in time-series manner (col. 3, lines 60-65), said first predetermined number of samples held being divided into a second predetermined number (4) of groups (refs. (1): "S13, S9, S5, S1", (2): "S14, S10, S6, S2", (3): "S15, S11, S7, S3", and (4): "S16, S12, S8, S4"); spreading code generating means for generating a spreading code sequence ("REFERENCE INPUT") for said despreading (col. 4, lines 19-25); correlation value calculating means provided respectively corresponding to said second predetermined number of groups each for calculating a correlation value between samples of a corresponding one of said second predetermined number of group and said spreading

code sequence (col. 4, lines 26-30; refs. 90, 92, 94, and 96); and output control means (fig. 1, ref. 80) for successively outputting in time-series manner respective correlation values output from respective ones of said correlation value calculating means as correlation values output from one system (fig. 2, Outputs of correlators 90, 92, 94, and 96). The sub-correlators (90, 92, 94, and 96) of figure 2 of Leibowitz are each identical to the correlator shown in figure 1 of Leibowitz (col. 3, lines 57-60). Therefore, the adder or output control means in figure 1 (ref. 80) is inherently contained in each of the sub-correlators in figure 2. Further, the output control means of each of the sub-correlators will successively output correlation values in a time series manner according to the cyclic updating of the signal sequence contained in each sub-correlator. For instance, each sub-correlator will output a new correlation value by the output control means as a new input signal is added to it, and the input signals are updated cyclically according to the ring counter (fig. 2, ref. 98).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakajima et al (US 5487083; hereafter "Nakajima") in view of Leibowitz.

Regarding claim 12, Nakajima discloses a mobile wireless terminal for digital radio communication according to figure 5 comprising: reception-related modem

(modulator – demodulator) means (14-16) for demodulating received digital data and signal processing means (19) for processing a signal received by said reception-related modem means to output the processed signal, said reception-related modem means including a digital matched filter (14 and 16) for despreading on reception side a received signal sequence having been spread on transmission side (inherent). Nakajima does not disclose that the digital matched filter is comprising (a) received signal holding means for successively holding a first predetermined number of samples among samples constituting said received signal sequence input in time-series manner, said first predetermined number of samples held being divided into a second predetermined number of groups; (b) spreading code generating means for generating a spreading code sequence for said despreading; (c) correlation value calculating means provided respectively corresponding to said second predetermined number of groups each for calculating a correlation value between samples of a corresponding one of said second predetermined number of group and said spreading code sequence; and (d) output control means for successively outputting in time-series manner respective correlation values output from respective ones of said correlation value calculating means as correlation values output from one system. However, Leibowitz does teach a digital matched filter comprising the limitations of (a) by figure 2. Leibowitz discloses a received signal ("DATA") holding means (refs. S1-S16) for successively holding a first predetermined number of samples among samples constituting said received signal sequence input in time-series manner (col. 3, lines 60-65), said first predetermined number of samples held being divided into a second predetermined number (four

groups) of groups (refs. "S13, S9, S5, S1", "S14, S10, S6, S2", "S15, S11, S7, S3", and "S16, S12, S8, S4"). Leibowitz thereby teaches a multiplexed digital filter which can be utilized to boost the overall speed of the digital correlator function (col. 3, lines 54-68). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a matched filter having a received signal holding means which is divided into a number of groups as taught by Leibowitz as the matched filter of Nakajima because it could be used to boost the overall speed of the correlation. Further, Leibowitz discloses the limitations of (b)-(d) as applied to claim 4 above.

Allowable Subject Matter

9. Indication of allowable subject matter is made regarding claims 1-3, 5-11, and 13-16.

10. In addition to the statement of the reasons for the indication of allowable subject matter set forth in the first office action hereby indicated as applicable to claims 1, 5-9, and 13-16, the following is a statement of reasons for the indication of allowable subject matter regarding claims 2-3 and 10-11:

The prior art of record fails to anticipate or obviate the second control means for cyclically activating the logic circuits at a predetermined timing to cyclically input samples of the received signal to the storage circuits as claimed.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art of record not relied upon above is cited to show the current state of the art with respect to digital correlators.

"74ACT323 8 Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins" (Datasheet; Fairchild Semiconductor, 1988).

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (571) 272-3055. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason M. Perilla
October 5, 2004

jmp

CHIEH M. FAN
PRIMARY EXAMINER